Claims

What is claimed and desired to be secured by Letters Patent is:

1. A hierarchal memory structure, comprising:

at least one active predecoder adapted to be shifted out; and

at least one redundant predecoder adapted to be shifted in.

2. The structure of Claim 1 further comprising at least one higher address predecoded line coupled to at least said redundant predecoder.

3. The structure of Claim 1, further comprising at least one lower address predecoded line coupled to at least said active predecoder and paired with said at least one higher address predecoded line.

4. The structure of Claim 1, further comprising at least one shift pointer adapted to shift in said redundant predecoder.

5. The structure of Claim 1, further comprising shift circuitry adapted to shift said active predecoder out and said redundant predecoder in.

6. The structure of Claim 5, wherein said active predecoder is adapted to fire for current address mapping.

7. The structure of Claim 5, wherein said redundant predecoder is adapted to fire for previous address mapping.

8. The structure of Claim 5, further comprising a shift line coupled to at least said shift circuitry.

9. The structure of Claim 5, further comprising an addrcurrent line coupled to at least said active predecoder.

10. The structure of Claim 5, further comprising an addrprev line coupled to at least said redundant predecoder.

11. A hierarchical memory structure comprising:

a synchronously controlled global element;

a self-timed local element interfacing with said synchronously controlled global element;

at least one predecoder adapted to fire for current predecoding; and

at least one predecoder adapted to fire for previous predecoding.

12. The memory structure of Claim 11, further comprising a redundant block communicating with at least one predecoder.

13. The memory structure of Claim 11, wherein said global element includes a global predecoder.

14. The memory structure of Claim 11, wherein said global element comprises at least one global decoder.

15. The memory structure of Claim 11, wherein said global element comprises at least one global sense amplifier.

16. The memory structure of Claim 11, wherein said local element comprises a plurality of memory cells forming at least one cell array.

17. The memory structure of Claim 11, wherein said local element comprises at least one local sense amplifier.

18. The memory structure of Claim 11, further comprising at least one predecoder line communicating with said predecoder adapted to fire for current predecoding.

19. The memory structure of Claim 11, further comprising at least one predecoder line communicating with said predecoder adapted to fire for previous predecoding.

20. A predecoder block used with a hierarchical memory structure, comprising:

a plurality of active predecoders adapted to fire for current predecoding;

at least one redundant predecoder adapted to fire for previous predecoding;

a plurality of higher address predecoded lines;

a plurality of lower address predecoded lines, wherein one higher address predecoded line is coupled to all said lower address predecoded lines; and

at least one shift pointer adapted to shift in said redundant predecoder.

21. A predecoder block used with a hierarchical memory structure, comprising:

at least one current predecoder adapted to fire for current address mapping;

at least one redundant predecoder adapted to fire for previous address mapping; and

shift circuitry adapted to shift said active predecoder out and said redundant predecoder in.

22. A method of providing redundancy in a memory structure, comprising:

shifting out a first predecoder block; and

shifting in a second predecoder block.

23. The method of claim 22, further comprising shifting predecoded lines coupled to said first and second predecoder blocks.

24. The method of claim 22, further comprising using shifting circuitry coupled to said first and second predecoder blocks.